

Appl. No. 10/673,310
Examiner: EVERHART, CARIDAD, Art Unit 2891
In response to the Office Action dated June 9, 2005

Date: September 9, 2005
Attorney Docket No. 10112951

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A test device for detecting alignment of active areas and memory cell structures in DRAM devices with vertical transistors, wherein the test device is disposed in a scribe line region of a wafer, comprising:

parallel first and second memory cell structures disposed in the scribe line region, each having a deep trench capacitor and a vertical transistor structure formed in a substrate;

an active area disposed between the first and second memory cell structures, wherein the active area overlaps the first and second memory cell structures a predetermined width; and

first to fourth conductive pads disposed on both ends of the first and second memory cell structures respectively.

Claim 2 (original): The test device as claimed in claim 1, wherein a first resistance is measured by the first and second conductive pads disposed on both ends of the first memory cell structure, and a second resistance is measured by the third and fourth conductive pads disposed on both ends of the second memory cell structure, and alignment shift (ΔW) of the active area and the first and second memory cell structures is estimated according to the first resistance, the second resistance, and the predetermined width.

Claim 3 (cancelled)

Claim 4 (original): The test device as claimed in claim 1, wherein the first to fourth conductive pads are made of polysilicon.

Claim 5 (original): The test device as claimed in claim 1, wherein the wafer further has a memory region including a plurality of memory cells with vertical transistors.

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Claim 6-8 (cancelled)

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